

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau(43) International Publication Date
17 July 2003 (17.07.2003)

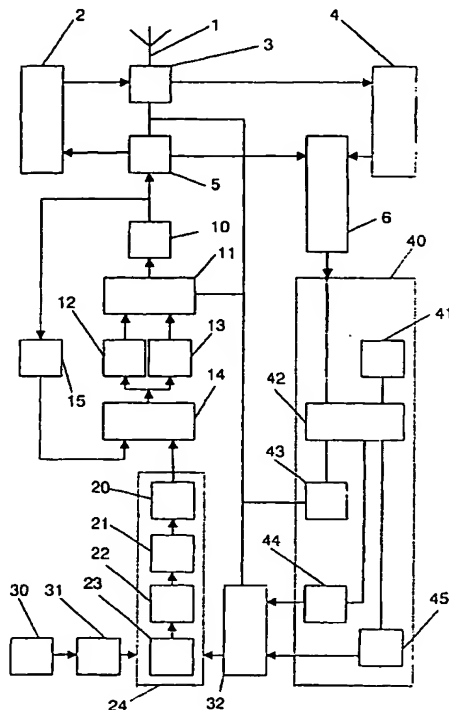
PCT

(10) International Publication Number
WO 03/058833 A1

- (51) International Patent Classification: H04B 1/40 (74) Agent: DULJVESTIJN, Adrianus, J.; Internationaal Octrooibureau B.V., Prof. Holstlaan 6, NL-5656 AA Eindhoven (NL).
- (21) International Application Number: PCT/IB02/05349
- (22) International Filing Date: 9 December 2002 (09.12.2002) (81) Designated States (*national*): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, OM, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.
- (25) Filing Language: English
- (26) Publication Language: English
- (30) Priority Data: 02075026.1 7 January 2002 (07.01.2002) EP
- (71) Applicant (*for all designated States except US*): KONINKLIJKE PHILIPS ELECTRONICS N.V. [NL/NL]; Groenewoudseweg 1, NL-5621 BA Eindhoven (NL).
- (72) Inventor; and (84) Designated States (*regional*): ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).
- (75) Inventor/Applicant (*for US only*): LIU, Jigang [CN/NL]; Prof. Holstlaan 6, NL-5656 AA Eindhoven (NL).

[Continued on next page]

(54) Title: TRANSCEIVER WITH MULTI-STATE DIRECT DIGITAL SYNTHESIZER DRIVEN PHASE LOCKED LOOP



(57) **Abstract:** Transceivers for use in time division telecommunication units like mobile phones and base stations can be produced at lower costs by, in a transmitting mode, switching the direct digital synthesizer (DDS 24) driven phase locked loop (PLL 10-15) into a modulating state and supplying a modulation signal to the DDS and switching in the PLL a first filter (12) allowing the generation of an improved modulated signal, and by, in a receiving mode, switching the DDS driven PLL into an oscillating state and supplying a non-modulation signal to the DDS and switching in the PLL a second filter (13) allowing demodulation with reduced phase noise. A transmitter part (2) and a non-transmitter part (4,6) share a single DDS driven PLL, based upon the basic idea of using important parts in low cost transceivers for both modes, instead of using different parts for different modes, and achieve a good performance.

WO 03/058833 A1

Best Available Copy